## Big and Fast Anti-Caching in OLTP Systems



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### **Online Transaction Processing**

## transaction-oriented small footprint write-intensive









## A bit of history...



#### OLTP Through the Years

# relational model





#### rise of the web



#### "end of an era"

2015

1993

#### Modern OLTP Requirements

# web-scale (big) high-throughput (fast)







### Thesis Motivation

## traditional disk-based architectures aren't fast enough newer main memory architectures aren't big enough





## Can we have mainmemory performance for arger-than-memory





#### Thesis Overview: Contributions 1. anti-caching architecture larger than memory datasets in main memory DBMS 2. anti-caching + persistent memory exploring next-generation hardware and **OLTP** systems







#### **Introduction Overview and Motivation** Anti-Caching Architecture Memory Optimizations Anti-Caching on NVM Future Work and Conclusions



#### outine





#### Disk-Oriented Architectures ) assumption: data won't fit in memory ) disk-resident data, main memory buffer pool for execution ) concurrency is a must transaction serialization and locks









#### 1E+10

**price per GB (\$)** 1E+02

#### 1E+00 1970 1973 1976 1979 1982 1985 1988 1991 1994 1997 2000 2003 2006 2009 2012



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## 1. DBMS buffer pool 2. distributed cache 3. in-memory DBMS









#### Buffer Poo

) must still... > maintain buffer pool b lock/latch data Maintain ARIES-style recovery logs all these things?



## ) question: What is the overhead of





#### 31%



**Buffer Pool** Locking Recovery **Real Work** 



26%

#### OLTP Through the Looking Glass, and What We Found There SIGMOD '08



## 1. DBMS buffer pool 2. distributed cache 3. in-memory DBMS













#### Persistence Layer









#### Main Memory Cache

# fast and scalable, but... key-value interface not ACID (AI, not CD)





#### **Consistency and Durability** ) reads are easy, writes are not > multiple copies of data > application's responsibility for OLTP, writes are common and consistency is essential







## 1. DBMS buffer pool 2. distributed cache 3. in-memory DBMS











#### H-Store Architecture ) partitioned, shared-nothing single-threaded main memory execution > no need for locks and latches blightweight recovery Snapshots + command log























## big: disk-oriented fast: memory-oriented big and fast: anti-caching



#### Big and Fast



## OLTP workloads are skewed





) asynchronous disk fetches > don't block ) maintain ordering of evicted data accesses ensures transactional consistency single copy of data Consistency is free ) efficient memory use, no swizzling



## Design Principles



#### **Introduction Overview and Motivation** Anti-Caching Architecture Nemory Optimizations Anti-Caching on NVM Future Work and Conclusions



#### outine



) memory is primary storage, cold cache done in 3 phases > avoids blocking, ensures consistency



## Architectural Overview data is evicted to disk-based anti-

#### reading data from the anti-cache is



## Anti-Caching Phases **EVICE** bre-pass JERGN **Merge**





#### 1. data > anti-cache threshold 2. dynamically construct anticache blocks of coldest tuples 3. asynchronously write to disk



evicted data is accessed of evicted blocks



## Pre-Pass 1. a transaction enters pre-pass when 2. continues execution, creating list 3. abort, queue blocks to be fetched





#### 1. data is fetched asynchronously from disk > avoids blocking 2. moved into merge buffer



## 



1. data is moved from in-memory restarted 3. transaction executes normally



## Merce merge buffer to in-memory table 2. previously aborted transaction is



done online, more responsive to changes in workload b goal is low CPU and memory overhead ) approximate ordering is OK

![](_page_35_Picture_1.jpeg)

# Tracking Access Patterns

![](_page_35_Picture_5.jpeg)

maintain LRU chain embedded in tuple headers ) per-partition are sampled randomly ) configurable sample rate

![](_page_36_Picture_1.jpeg)

## Approximate LRU (aLRU)

# ) transactions that update LRU chain

![](_page_36_Picture_5.jpeg)

#### Anti-Caching vs. Swapping > fine-grained eviction blocks constructed dynamically ) asynchronous batched fetches > possible because of transactions

![](_page_37_Picture_1.jpeg)

![](_page_37_Picture_3.jpeg)

Anti-Caching vs. Caching ) data exists in exactly one location caching architectures have multiple copies, must maintain consistency ) data is moved, not copied ) goal is increased data size, not throughput

![](_page_38_Picture_1.jpeg)

![](_page_38_Picture_3.jpeg)

#### Benchmarking **VCSB** Zipfian skew > data > memory ) read/write mix MySQL, MySQL + memcached

![](_page_39_Picture_1.jpeg)

![](_page_39_Picture_3.jpeg)

#### YCSB, read-only, data 8X memory anti-cache MySQL - MySQL + memcached

120000

S (txn/ throughput

![](_page_40_Figure_3.jpeg)

![](_page_40_Picture_4.jpeg)

workload skew (high -> low)

41

#### YCSB, read-heavy, data 8X memory anti-cache MySQL - MySQL + memcached

![](_page_41_Figure_1.jpeg)

S txn throughput

![](_page_41_Figure_3.jpeg)

![](_page_41_Picture_4.jpeg)

![](_page_41_Figure_6.jpeg)

![](_page_41_Picture_7.jpeg)

![](_page_41_Picture_8.jpeg)

#### Tracking Accesses Revisited ) approximate ordering is OK > original implementation ) alru (linked list) ) compute vs. memory Can we reduce the memory overhead?

![](_page_42_Picture_1.jpeg)

![](_page_42_Picture_2.jpeg)

![](_page_42_Picture_3.jpeg)

#### Timestamp-Based Eviction > use relative timestamps to track accesses ) to evict, take subset of tuples and evict based on timestamp age ) questions: ) timestamp granularity sample size (power of two)

![](_page_43_Picture_1.jpeg)

![](_page_43_Picture_3.jpeg)

#### Timestamp Granularity 14 byte timestamps > use instruction counter > 2 byte timestamps ) use epochs, set the timestamp to the current epoch

![](_page_44_Picture_1.jpeg)

![](_page_44_Picture_4.jpeg)

![](_page_44_Picture_5.jpeg)

![](_page_45_Figure_0.jpeg)

![](_page_45_Picture_1.jpeg)

![](_page_45_Picture_4.jpeg)

#### Key Take-Aways **8-17X improvement for** skewed workloads at largerthan-memory data sizes ) disk becomes the bottleneck for lower skew

![](_page_46_Picture_1.jpeg)

![](_page_46_Picture_2.jpeg)

47

![](_page_46_Picture_4.jpeg)

#### Hardware Assumptions are Key heavily influence system architectures ) many factors **Capacity b atency volatility**

![](_page_47_Picture_1.jpeg)

![](_page_47_Picture_3.jpeg)

#### What's next for OLTP?

![](_page_48_Picture_1.jpeg)

## Non-Volatile Memory

![](_page_49_Picture_1.jpeg)

![](_page_49_Picture_3.jpeg)

#### Properties of NVM > non-volatile ) random-access high write endurance ) except flash byte-addressable ) except flash

![](_page_50_Picture_1.jpeg)

#### The NVM Arms Race FERAM high write endurance **MRAM DRAM-like latency** PCM (PRAM) **DRAM-like capacity**

![](_page_51_Picture_1.jpeg)

52

![](_page_51_Picture_4.jpeg)

**OLTP architectures and NVM** > anti-cache architecture disk-based architecture ) open questions What adaptations are needed?

![](_page_52_Picture_1.jpeg)

# Looking Forward...

## Which architecture is best suited for NVM?

![](_page_52_Picture_5.jpeg)

#### ) goal: provide product-independent analysis test wide range of latency profiles ) automatically add specified latency built by collaborators at Intel

![](_page_53_Picture_1.jpeg)

#### Anti-Caching on NVM replace disk with NVM > several adaptations necessary Iightweight array-based anti-cache ) utilizes mmap interface fine-grained block and tuple eviction interface

![](_page_54_Picture_1.jpeg)

![](_page_54_Picture_3.jpeg)

#### Disk-Oriented Architectures on NVM

#### ) must adapt both storage and log files to be use NVM mmap interface configure to use fine-grained buffer bool bacles

![](_page_55_Picture_2.jpeg)

![](_page_55_Picture_4.jpeg)

![](_page_56_Figure_0.jpeg)

![](_page_56_Picture_1.jpeg)

![](_page_56_Picture_5.jpeg)

#### YCSB, read-heavy, data 8X anti-caching MySQL

180000

(S txn throughput

![](_page_57_Figure_3.jpeg)

![](_page_57_Picture_4.jpeg)

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![](_page_57_Picture_7.jpeg)

## Future Work

![](_page_58_Picture_1.jpeg)

#### Multi-Tier Architectures DRAM -> NVM -> Disk/SSD ) open questions indexing structures > synchronous/asynchronous fetches

![](_page_59_Picture_1.jpeg)

![](_page_59_Picture_3.jpeg)

![](_page_59_Picture_4.jpeg)

#### Anti-Caching Indexes ) index size can be significant > can cold index ranges be evicted to an anti-cache? bopen questions how/what to evict ) execution changes

![](_page_60_Picture_1.jpeg)

![](_page_60_Picture_3.jpeg)

#### Semantic Anti-Caching Current implementation makes no assumption about types of skew Skew typically as semantic meaning e.g., temporal, spatial ) can we leverage these domain

semantics?

![](_page_61_Picture_2.jpeg)

![](_page_61_Picture_3.jpeg)

![](_page_61_Picture_4.jpeg)

![](_page_62_Picture_0.jpeg)

#### > anti-caching architecture outperforms and outscales previous OLTP architectures > well-suited for next-generation NVMbased architectures

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#### Conc usions

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![](_page_63_Picture_10.jpeg)

![](_page_63_Picture_11.jpeg)

![](_page_63_Picture_12.jpeg)

![](_page_63_Picture_13.jpeg)

#### Ouestions?

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